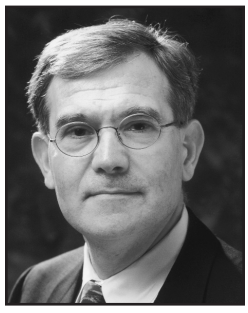
Session 1 Overview

Plenary Session



Chair: *Timothy Tredwell, Eastman Kodak, Rochester, NY*
Chair, ISSCC Executive Committee

Associate Chair: *Jan Van der Spiegel, University of Pennsylvania, Philadelphia, PA*
Chair, ISSCC International Technical-Program Committee

The Plenary Session begins with formal opening remarks by the Executive- Committee Chair, Tim Tredwell. At the end of his general welcome, he introduces the first of three Plenary presenters. Following the first Plenary Talk, there will be a presentation of Awards given by ISSCC, SSCS, and the IEEE. After a short break, the second and third Plenary Talks will be given. Overall, the Plenary Talks will provide a range of perspectives on this year's Conference Theme: "The 4 Dimensions of IC Innovation". The theme underscores the increasing interaction, in the nano-scale era, between the various traditionally-isolated aspects of Solid-State Circuit realizations, namely, Technology, Devices, Circuits, and System Architecture. Deep understanding of manufacturing technologies and the impact of physical device limitations on circuit and system performance is becoming essential for continued innovation within the IC industry.

The first Plenary Talk is by Morris Chang, Founding Chairman of the Taiwan Semiconductor Manufacturing Company (TSMC). He will deal with the importance of the silicon-foundry in the continued health of the overall IC industry. In his talk, he will review the challenges that the foundry-industry must overcome in ensuring continued growth. He will focus on the need for growth and profitability in an increasingly competitive environment. He proposes ways to deal with these challenges by expanding into new IC markets, and by penetrating other ones that are currently not using IC foundry services. To ensure success of this thrust, a new type of foundry-customer relationship is going to be necessary, one that allows design and technology cooperation to proceed hand-in-hand from the early stage of product development, in order to meet increasingly complex product requirements.

The second Plenary Talk is by Lewis W. Counts, Vice-President of Technology and Fellow at Analog Devices. He will focus on the importance of interactions between technology, circuits, systems, and applications, in analog and mixed-signal electronics. He observes that the move into deep-submicron CMOS technology has increased the role of analog and mixed-signal circuit design in the continued growth of the IC industry. Now, exploiting the process technology has become essential also in the digital world in order to minimize the influence of process variations on product performance. In support of his view that historical development in analog and mixed-signal illuminate the path for digital adaptation, He will illustrate the importance of a number of developments in analog and mixed-signal subsystems for a variety of high-speed communication systems. Their success typically depends on analog and mixed-signal circuits that are able to work within low supply voltages while maintaining their dynamic range through new circuit innovation. He observes that such innovations depend more and more on the creative combination of process, and design with system architecture.

The third Plenary Talk is by Joël Hartmann, Director of the Crolles2 Alliance and STMircoelectronics. He will focus on a new "Nanoelectronic Cosmology" in which tightly-coupled modeling and simulation of physical, electrical, mechanical, and process aspects of product solutions have become essential for predicting the impact of design choices on product performance. Currently, devices in the nanometer regime display significant parameter variability, leading to an increasingly serious mismatch between early simulation and ultimate measurement. A better understanding of the physical causes of this mismatch is required to ensure acceptable levels of performance, manufacturability, and yield. As a vehicle for change, he proposes the concept of Generalized Design-for-Manufacturability (GDFM) that unifies Design-for-Manufacturability, Manufacturing-for-Design, and Design-for-Yield, which bring together the four dimensions of IC innovation into a new Nanoelectronic Cosmology.

1.1 Foundry Future: Challenges in the 21st Century **8:40 AM**

Morris Chang, Founding Chairman, Taiwan Semiconductor Manufacturing, Hsinchu, Taiwan

The dedicated-foundry industry was established in 1987, with the incorporation of Taiwan Semiconductor Manufacturing Company (TSMC). Silicon-wafer production at foundries has increased significantly since that time, to account for over 20% of all wafer volume; Foundries are now an integral part of the overall semiconductor supply-chain. There is every reason to anticipate that the importance of the foundry industry will increase further: We believe that the foundry business-model is an important positive influence on the health of the overall IC industry. Accordingly, it is critically necessary to scan the future for potential issues that might inhibit foundry-industry growth. We see two significant challenges that the foundry industry must address, in order to ensure its continued expansion:

The first and foremost challenge is business growth: We anticipate that growth matching previous industry experience may be more difficult to attain in the future, simply because revenue growth of the semiconductor IC industry (as a whole) has slowed since 2000. Prior to this, the average industry growth-rate was 16%, but, over the period 2000 to 2010, the growth rate will slow to 6%. Additionally, the penetration of the CMOS-logic market by the foundry industry cannot continue unabated indefinitely; saturation should be anticipated in the future.

The second challenge for the foundry industry is to maintain profitability: The growth of the industry has attracted many companies to offer foundry services. Consequently, competition between these companies increases the potential for commoditization of foundry services, where many foundries, with apparently similar (but substantively different) services, compete on the basis of price alone.

We believe that the foundry industry must respond to these challenges by two means: expanding into new IC-product markets enabled by the cost reduction and performance increases resulting from technology scaling; and by penetrating segments of the IC market that are currently not involved in foundry relationships, by broadening the range of technologies that are offered. In the future, circuit designers can expect, therefore, to be able to access process technologies tuned in various ways: For memory, analog, high-performance-logic, or image-sensor applications, as well as for CMOS logic.

The foundry company must develop strategies to avoid commoditization! In our opinion, one of the most important aspects of the foundry response to commoditization must be to create a much deeper and broader relationship between the foundry and each of its customers. This new type of integrated relationship differs from many previous foundry–customer relationships, in that both design and technology engineering proceed concurrently from an early stage in the product-development effort. Note that the success of this relationship will require a much greater information flow between the design and foundry teams, and optimization of both design and process technology to meet product requirements. Such relationships can offer a significant advantage to customers in meeting product-cost, performance, and time-to-market requirements.

1.2 Analog and Mixed-Signal Innovation: The Process-Circuit-System-Application Interaction **10:15 AM**

Lewis W. Counts, Vice-President of Technology and Fellow, Analog Devices, Wilmington, MA

Innovation in analog and mixed-signal electronics becomes increasingly more important to the continued growth of the IC industry. Technologists working in the analog and mixed-signal arena certainly share, with their digital counterparts, the overarching goal of reducing power and cost-per-function in each IC generation; But they must also operate under physical constraints that, until recently, have been secondary in the digital world. From the advent of the first analog IC, analog designers have exploited the potential of the process technology to develop circuits that minimize the impact of variation in process parameters on product performance. The bandgap reference is just one example. More generally, trim, calibration, and circuit techniques such as charge-redistribution, enabled economic production of amplifiers and data converters with 12-bits (or better) precision on “8-bit” processes. In addition, while process scaling has enabled the development of a wide variety of products, from cell-phones to advanced medical-imaging systems, the success of these products depends in large measure on their ease of use, and seamless connection to wireless and wired networks. Analog and mixed-signal subsystems, including display drivers, and WLAN and cellular radios, support these critical interfaces. The downward scaling of supply voltage in deep-submicron CMOS (now at 1V), may limit dynamic range, forcing some analog functions to be implemented on other processes, but it has also enabled new circuit architectures that gain back dynamic range.

The creative combination of process, design, and system architecture in providing robust solutions for demanding applications, will prove to be even more crucial in the future. Such solutions will be essential in meeting the challenges posed by the physical realities of deep- submicron design in achieving gigahertz speeds, minimizing power- consumption, and integrating multiple functions in smaller packages.

1.3 Toward A New Nanoelectronic Cosmology **11:05 AM**

Joël Hartmann, Director, Crolles2 Alliance, STMicroelectronics, Crolles, France

Gone forever, are the days of smooth roadmap scaling, with its more-or-less-simple design rules, adequate supply voltages, and unimpeded circuit shrinkage. As scaling moved ahead to nanometer dimensions, things changed: Devices became more difficult to predict, and global performance degraded due to leakage and dispersion. One of the consequences of this deteriorating situation has been that increased parameter variability has led to a significant mismatch between simulation and actual-measurement results, at all levels. While many of these effects have been already well-known to analog designers, the surprise, now, is that they are more broadly important, even in digital design, where previously available noise margins have almost disappeared. Clearly, deep understanding and modeling of all underlying physical causes is urgently required to guide the right choices at all levels. Conceptually, such understanding will lead to acceptable levels of performance, manufacturability, and yield, at ever-decreasing feature sizes. Meanwhile, the increased parameter variability observed today, as one technology node invites the next, reveals the tight coupling of the four seemingly- independent dimensions of design, motivating the need to configure a new nano-cosmology, one in which global optimization results only from an intricate balance between the Process, Device, Circuit, and System aspects of design. In this new nano-cosmology, the emerging concept of Generalized Design-for-Manufacturability (GDfM) unifies current Design-for- Manufacturability (DfM), Manufacturing-for-Design (MfD), and Design-for-Yield (DfY), coupling all of the above-mentioned dimensions within a new space where their inter-dependence is revealed and exploited. Tightly-coupled physical-electrical-mechanical-process modeling and simulation, will allow early detection of the impact of design choices at all levels. This creates a 4D knowledge continuum reminiscent of the ideas of General Relativity, ones extremely rich in consequences for the future of nanoelectronic design.